Highly Accelerated Life Testing (HALT) of K-4500 Low Fired X7R Dielectric *

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Abstract

Highly accelerated life test was performed on an 0805 – 100 nF X7R multilayer chips with 12 microns active layer thickness. The material is a low fired commercial product (SF-422) produced by MRA Laboratories, with a dielectric constant of about 4500.

The test conditions consisted of 125, 140, 155, and 175°C, and voltages ranging between 250 and 600 volts. The preliminary data showed a temperature dependence of an activation energy of 1.21 electron volt, nearly similar to that reported by other researchers on an X7R – $BaTiO_3$ system. However, the voltage dependence of acceleration factor (n) was found to be in the range of 5.4 to 7.1, almost twice as large as those reported in the literature. The experimental data showed a good fit with the Weibull statistical distribution. These observations suggest that this dielectric should be useful for high voltage and high temperature applications.

For this type of MLC chip, tested at twice rated voltage (100V, 125°C), the mean life time was predicted to be in excess of one million hours.

INTRODUCTION

We recently reported[1] on the physical and electrical properties of a high K (4500), low fired, barium titanate base X7R dielectric. This material is commercialized as product SF-422.

The shift in market demands for higher voltage (>200V) and higher temperature (>125°C) X7R applications have prompted us to examine the intrinsic capability of this dielectric for these applications. As a first phase of this study, we performed a highly accelerated life testing (HALT) in the temperature range of 125 to 175°C and voltage range of 250 to 600 volts on 0805-100nF chips with fired layer thickness of about 12 microns.

Accordingly, the objective of this paper is to report the HALT results on this dielectric.

Prokopowicz and Vaskas were the first to use an empirical relationship to predict the mean time to failure of multilayer ceramic capacitor, based on accelerated life testing at higher voltage and temperature.

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n \exp\frac{E_a}{K}\left[\frac{1}{T_1} - \frac{1}{T_2}\right] \qquad (1)$$

Where:

t_1 = the mean time to failure at V_1 and T_1
t_2 = the mean time to failure at V_2 and T_2
V_1, V_2 = test voltages of the MLC, in Volts
T_1, T_2 = test temperatures of the MLC in °K
n = voltage stress exponent
E_a = activation energy (electron-volt)
K = Boltzman constant = 0.86×10^{-4}ev/°K

Based on the results observed by many researchers, this equation appeared to fairly predict the life expectancy of the capacitor and is widely used in the industry to assess the properties of the MLC capacitors.

For $BaTiO_3$ based MLC chips, Prokopowicz[2] reported a value of 2.7 for n and 0.9 ev for activation energy E_a.

Other researchers have reported slightly different values. Very recently, however, Sakabe [9] reproted a voltage acceleration factor that ranged between 5.5 and 6.9 for Y-doped X7R $BaTi0_3$ dielectric. The HALT data were generated on MLC, with very thin active layers around 2 microns and Ni internal electrode. The Table I below summarizes their findings.

Table I

Dielectric System	n	E_a(ev)	Reference
$BaTiO_3$–X7R	2.7	0.9	Prokopowicz (2)
$BaTiO_3$–X7R, Z5U	3.0	1.0	Munikoti (3)
$BaTiO_3$-Z5U	2.46	1.19	Minford (4)
High K	2.5	1.0	Kurtz (5)
$BaTiO_3$-X7R	3.0	1.15	Confer (6)
Y-doped $BaTiO_3$ with Ni-electrode	3.0	1.4	Sato (7)
$BaTiO_3$-Y5V with Ni-electrode	3.6	1.2	Pak and Rawal (8)
PMN	5.5 to 5.9	1.1 to 1.2	Pak and Rawal (8)
Y-doped $BaTi0_3$ with Ni-electrode	5.5 to 6.9	1.1 to 1.3	Sakabe (9)

The Values generally used in the industries are: n=3 and E_a=1.1 ev.

During our research, we were surprised to find that the voltage acceleration exponent n, was greater than 5, however the average activation energy E_a was 1.21 ev and it is within the reported range shown in Table I.

EXPERIMENTAL SAMPLE

MLC capacitors of 0805 size with 30 layers of about 12 microns fired thickness were manufactured by the "wet" deposition process in our laboratories. The internal electrode was 70 Ag/30 Pd composition.

* Presented in parts at the U.S. – Japan Seminar, Nov. 1999, Okinawa, Japan

The sample used for this study was taken from a single firing representing about 20,000 chips. After silver termination, the chips were measured for capacitance and dissipation factor, and all showed 100 nF ± 5%. No other testing was done prior to the HALT study. The pertinent physical and electrical properties of this sample are shown in Table II. The temperature coefficient of capacitance (TCC) and SEM image of a polished cross section are shown in figures 1 and 2, respectively.

Table II

- Sintering Temperature: 1130°C/3 hour
- Fired Density Ceramic only 5.85 g/cm^3 (97.5% of theoretical)
- Size: 0805 (2.0 x 1.25mm)
- Number of Layers: 30
- Fired Layer Thickness: 12 microns
- Average Capacitance at 1 KHz, 1 Vrms, 24 hours: 101 nF
- Average Dissipation Factor: 1.8%
- Calculated Dielectric Constant "K": 4600

HALT SETUP

A test fixture was assembled to accommodate 24 individual chips held in place by a spring loaded strip. The temperature chamber is a Blue-M oven Model OV-490A-1. The test temperature was held to ± 2°C from the set value. A 1000 Ω resistor and a relay were connected in series with each capacitor. The leakage current of each capacitor was monitored during the test. The test circuit was interphased with a PC which recorded the exact time of failure on each chip. When the leakage current exceeded 10^{-5} ampere, the relay opened up, thus removing the failure from the test and the time was recorded by the PC. The power supply is a KepCo Model 2000M where the voltage was held to ±1 volt from the set value.

TEST RESULTS

Although many researchers have used lognormal and Weilbull statistics to analyze the HALT data, in this study we used the Weilbull to determine the mean time to failure at 63% failure level of the test samples. Table III below shows the different test conditions that were used. 22 chips were tested at each condition until more than 90% of the sample had failed.

Table III

Life Test Conditions

Temperature °C	125	140	155	175
Voltages (Volt)	500	450	350	250
	550	500	400	300
	600	550	450	350

Figures 3, 4, 5 and 6 show the Weibull plot curves for 175, 155, 140 and 125°C for three different voltages, respectively. The early failures (below 30%) were considered to be caused by manufacturing defects such as thin spots in the active layers. The mean time to failure at 63% failure level for each test condition was determined from the graphs with the help of a MathCad program and curve fit linear regression statistic.

Using equation (1), the voltage acceleration factor n, and the activation energy E_a were determined for the various test conditions as shown in Figures 7 and 8, respectively.

It is interesting to note that a higher n (>6) was observed for test temperatures at 155 and 175, while for 125 and 140°C conditions, n was between 5.4 and 5.7.

Similarly the activation energy of failures was higher (E_a = 1.35 ev), for higher stress voltage 550V than for 300V, with an E_a = 1.1 ev.

PREDICTED VERSUS ACTUAL TIME TO FAILURE

Using an average voltage stress, n = 6.17, and an average activation energy, E_a = 1.21 ev, the predicted time to failure at 63% failure level was compared to the actual time observed in this study. The time to failure, t_2, at T_2 = 175°C, and V_2 = 350, were used to generate the data shown in Table IV.

As can be seen from the results, the predicted TTF at 125 and 140°C are somewhat lower than the actual values while for 155 and 175°C, the actual TTF values, are slightly lower than the predicted one. These differences can, perhaps, be explained by slight variation in test temperature.

Assuming we can further predict the TTF of these chips at 100V and 125°C, which corresponds to twice rated voltage, the life time will be greater than 10^6 hours (114 years).

Table IV

Examples of Time to Fail (TTF) Predictions
Based on the data for 175°C, 350 Volt case:
n = 6.17 (Average), Activation energy = 1.21 ev. (Average)
P = predicted TTF, A=actual TTF (at 63% Failed)

Oven temperature has a strong effect on the predictions. For example, the 125°C, 550 volt case would be 133 hours at 123°, and 93 hours at 127°, instead of 111 hours at 125°

Predicted TTF vs Actual TTF (Hours)								
Temp	125		140		155		175	
Volts	P	A	P	A	P	A	P	A
50	$3*10^8$							
100	$4*10^6$							
250							279	299
300				+	393	365	91	86
350					152	156	xxx	35
400					67	45		
450			10	148				
500	200	27	55	74				
550	111	18	31	45				
600	65	90						

ULTIMATE DIELECTRIC BREAKDOWN VOLTAGE

To gain further insight into the capability of this dielectric, we have also performed a voltage breakdown analysis on a 22 chip size sample at 25,

125, 140, 155 and 175°C. The HALT fixture was used for this test. The voltage was raised slowly (about one minute) on each chip, until failure (relay opened). The failures distribution are shown in Table V.

Table V

Ultimate Dielectric Breakdown at Different Temperatures

Temperature °C	25	125	140	155	175
Minimum Voltage (Volts)	735	603	855	782	535
Maximum Voltage (Volts)	1120	990	1074	1140	1137
Average Voltage (Volts)	939	857	980	965	989

It is interesting to note that the ultimate dielectric breakdown remained relatively high even to 175°C. Further work will be performed with increase in temperature to 300°C.

SUMMARY

- A HALT analysis was performed on 0805, 100 nF chips, of a low fired K-4500 X7R dielectric, between 125 and 175°C, and voltage stress ranging from 250 to 600 volts, on 12 microns layer thickness.
- The voltage acceleration exponent, n, ranged between 5.4 to 7.1, while the activation energy, E_a, ranged between 1.1 and 1.35 electron-volts.
- The insulation resistance on test was monitored and remained relatively high $>10^8$ ohms and constant until breakdown (thermal runaway).
- The ultimate dielectric breakdown voltage remained relatively high, >75V/micron even to 175°C.
- Using the time to failure value generated at 175°C and 350V, and averages n = 6.17, and E_a = 1.21 ev, the predicted life time was in close agreement with actual values at the lower test temperatures and higher voltage.
- Assuming that the average n and E_a generated in this study to be valid, the predicted life time of the 0805, 100 nF chip will be:
  at 100V, 125°C : 4×10^6 hours
  and at 50 V, 125°C: 3×10^8 hours

ACKNOWLEDGEMENT

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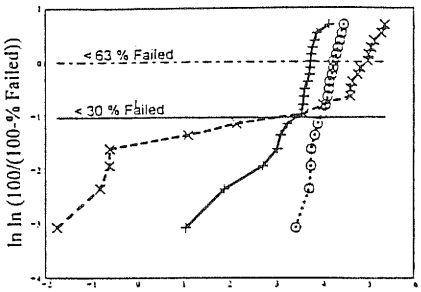
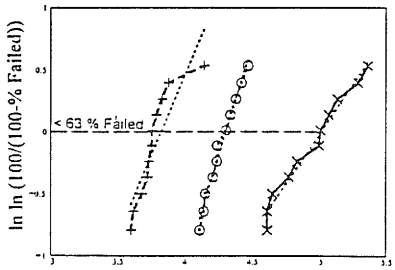


Figure 5 - Weibull Plots of 140 Degree C Data

X - 450 Volts
O - 500 Volts
+ - 550 Volts



Slopes of 140 C Data > 30 % Failed

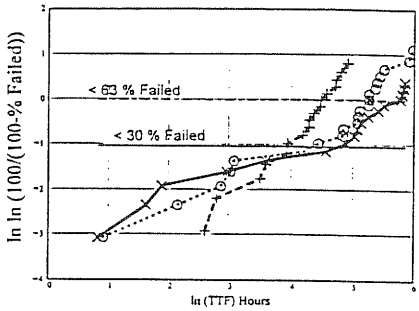
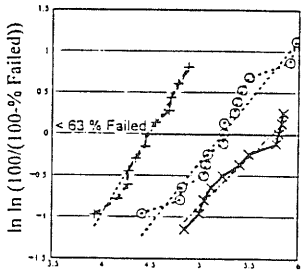


Figure 6 -Weibull Plots of 125 Degree C Data

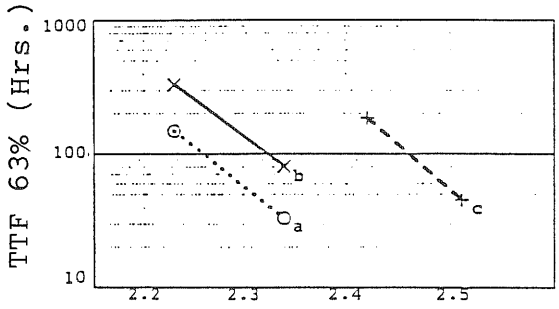
X - 500 Volts
O - 550 Volts
+ - 600 Volts



Slopes of 125 C Data > 30% Failed

Figure 7 - Voltage Acceleration Factor, n

Figure 8 - ACTIVATION ENERGY, E_a

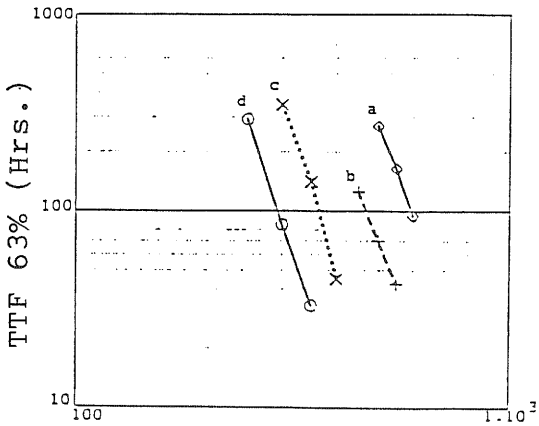


1/T; per degree K * 10^3

O - 300 Volts, 1.1 ev a

X - 350 Volts, 1.17 ev b

+ - 550 Volts, 1.35 ev c



VOLTS

125° C, n = -5.7 a

140° C, n = -5.4 b

155° C, n = -7.1 c

175° C, n = -6.5 d

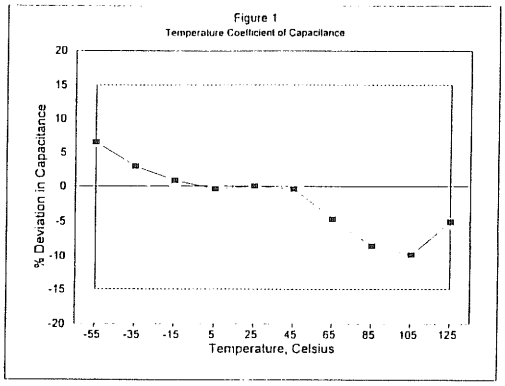
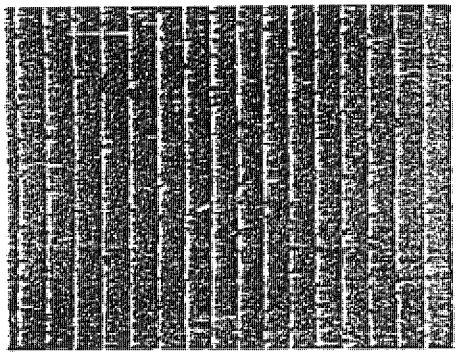


Figure 2
Polished Cross-section

Bar Marker = 10 Micro Meters



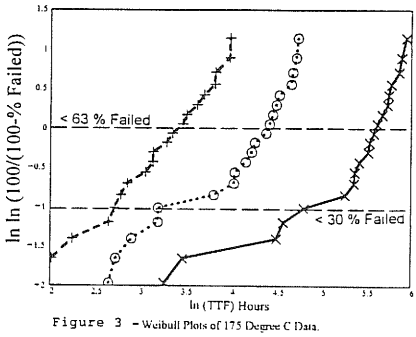


Figure 3 - Weibull Plots of 175 Degree C Data.
X - 250 Volts
O - 300 Volts
+ - 350 Volts

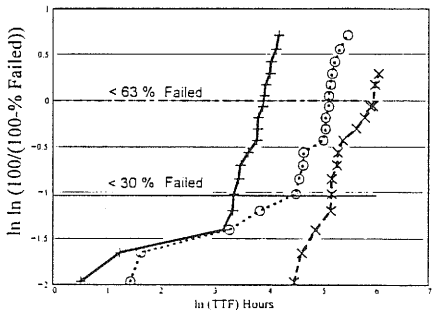
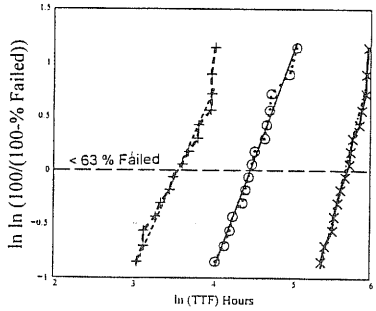
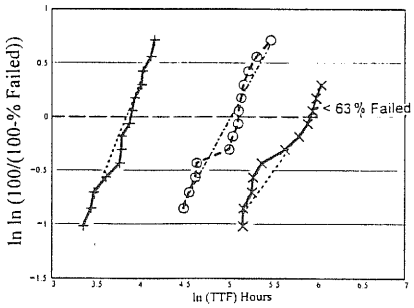


Figure 4 -Weibull Plots of 155 Degree C Data
X - 300 Volts
O - 350 Volts
+ - 400 Volts



Slopes of > 30% Failed Data, 175 C



Slopes of > 30% Failed Data, 155 C

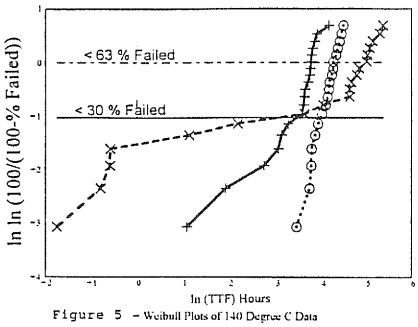
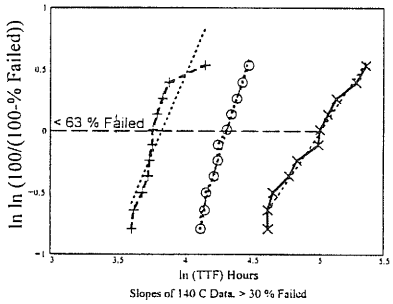


Figure 5 - Weibull Plots of 140 Degree C Data

X - 450 Volts
O - 500 Volts
+ - 550 Volts



Slopes of 140 C Data, > 30 % Failed

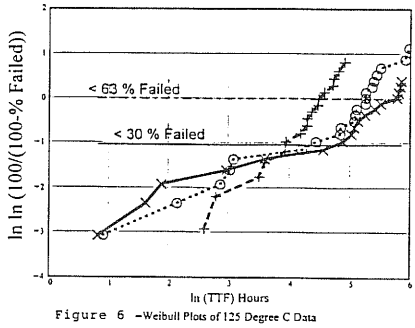
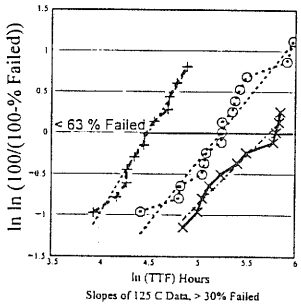


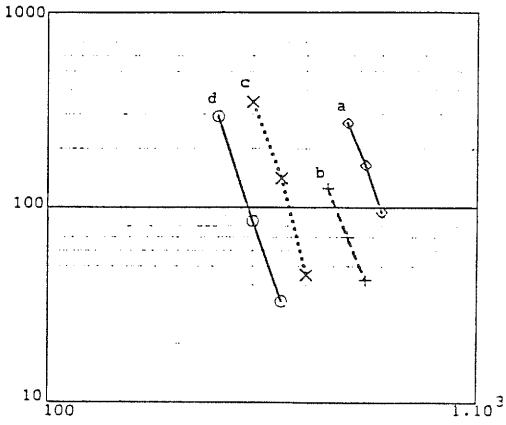
Figure 6 -Weibull Plots of 125 Degree C Data

X - 500 Volts
O - 550 Volts
+ - 600 Volts



Slopes of 125 C Data, > 30% Failed

Figure 7 - Voltage Acceleration Factor, n



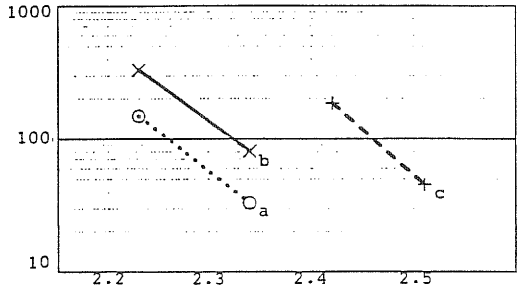
125° C, n = -5.7 a

140° C, n = -5.4 b

155° C, n = -7.1 c

175° C, n = -6.5 d

Figure 8 - ACTIVATION ENERGY, E_a



1/T; per degree K * 10^3

O - 300 Volts, 1.1 ev a

X - 350 Volts, 1.17 ev b

+ - 550 Volts, 1.35 ev c