RoHS Compliant Very Low Fired High-K (K~100) COG Dielectric for Air Fired Multilayer Ceramic Capacitors

Anton V. Polotai, Samir G. Maher, James M. Wilson and Riad G. Maher

MRA Laboratories, Inc.
15 Print Works Drive, Adams, MA, 01220
Tel: (413) 743-3927, Fax: (413) 743-0305, E-mail: mra@mralabs.com
www.mralabs.com

Abstract

High-K linear dielectrics, compatible with precious metal electrodes (PME), are widely used in medical, aerospace and military niche applications, where the necessity of stable electrical performance under high power, high frequency and high temperature conditions is of the utmost importance. The PME capacitor industry constantly demands new linear dielectrics with a higher dielectric constant and lower sintering temperatures for product range extension and cost reduction. Currently, there are only a few commercial Class-1 COG dielectrics available on the market with a dielectric constant above 90 and compatible with 95%Ag/5%Pd or 90%Ag/10%Pd internal electrodes. The recently adopted Restriction of Hazardous Substances (RoHS) regulation further reduced the selection of available dielectric materials. This paper describes a newly developed, very low fired, and RoHS compliant high-K (K~100) COG dielectric, VLF-101, which is compatible with 95%Ag/5%Pd electrode system. Basic electrical properties of the new dielectric were evaluated based on performances of multilayer capacitors with varied dielectric layer thicknesses.

Introduction

Value-added and application specific ceramic capacitor markets are dominated by low volume and higher priced components, where cost is considered secondary to product performance. These markets include aerospace, military and medical niche applications, specialty power supplies, under-the-hood automotive electronics, downhole pumps and many others. In spite of a relatively small market share, about 10-15% of the total market of ceramic capacitors, the markets of value-added and application specific ceramic capacitors are considered to be very attractive due to overall stability and high profit margins [1]. A majority of multilayer ceramic capacitors (MLCCs) for these applications are manufactured using traditional air fired ceramic dielectric materials in conjunction with precious, silver-palladium, metal electrodes. Contrary to the base metal electrode (BME) MLCC market, where the main driving forces are overall price reduction and increase of volumetric efficiency of MLCC chips, specialty PME MLCCs are generally manufactured with thicker dielectric layers, ranging from about 5µm to about 100µm or more. Thick dielectric layers are required to ensure unprecedented stability of electrical properties at specific operation conditions for a required period of time. For example, according to the MIL-PRF-123 specification, military grade PME ceramic capacitors with high reliability should have a minimum dielectric thickness of 20µm for 50 volt rated capacitors, or 25µm for capacitors with rated voltage above 50 volts [2].

The PME capacitor industry is in constant demand for new ceramic dielectric materials with higher dielectric constant, lower sintering temperatures and improved reliability for product range extension and cost reduction. Reduction of sintering temperature of the dielectric material allows the substitution of very expensive palladium (Pd) with less expense silver (Ag) in internal electrodes. It also facilitates the decrease of overall equivalent series resistance (ESR) of the device due to the higher electrical conductivity of silver. In order to reduce the palladium content in the electrodes from traditional 30% down to at least 5%, the sintering temperature of the dielectric has to

be reduced from 1100-1130°C down to 960-975°C. Simultaneous reduction of the dielectric sintering temperature and improvement of its electrical performance is not a trivial task. In most PME dielectric compositions, sintering fluxes, responsible for dielectric densification, have lower dielectric constant and higher electrical conductivity compared to the main dielectric phase [3]. Simple increase of the flux content may negatively affect electrical properties of the dielectric composition, so the entire dielectric formulation has to be carefully redesigned. Moreover, recently adopted Restriction of Hazardous Substances (RoHS) regulations restrict the use of lead, cadmium and four other hazardous materials in manufacturing various types of electronic components, significantly reducing the selection of available dielectric materials on the market. For example, due to high dielectric polarizability and compatibility with barium, lead was widely used in dielectric compositions with high dielectric constant, while cadmium was very effective in sintering fluxes [4, 5].

MRA Laboratories, Inc., a leading manufacturer of PME formulated ceramic dielectric materials for specialty applications, offers a broad line of Class-I COG and Class-II X7R/X8R/BX type dielectrics with a wide range of dielectric constant. In our previous report [6], we described a recently developed, RoHS compliant, and very low fired COG dielectric, VLF-085, with a dielectric constant around 82, capability to sinter at 1000°C and compatibility with 90%Ag/10%Pd electrode system. This paper reviews another newly developed RoHS compliant and very low fired COG dielectric, VLF-101, with a dielectric constant around 100. This dielectric has the capability to sinter at 960°C and is compatible with 95%Ag/5%Pd electrode systems. The properties of VLF-101 at variable temperatures and electric fields were evaluated based on the performance of .0805-size MLCC chips made with 95%Ag/5%Pd internal electrodes and three different dielectric layer thicknesses: 10µm, 20µm, and 45µm.

Experimental

VLF-101 is a newly developed, air fired, high-K (K~100) COG dielectric formulation, which complies with RoHS requirements for environmentally friendly "Green" materials. This dielectric, developed and manufactured by MRA Laboratories, Inc., is based on a modified pseudo-tungsten bronze-type $Ba_{6-3x}R_{8+2x}Ti_{18}O_{54}$ (R: rare earth elements) solid solution, modified in a way to reduce the amount of expensive neodymium oxide which is traditionally used in these types of dielectric compositions [3]. The initial powder properties of VLF-101 are summarized in Table 1.

Table 1. Initial powder properties of VLF-101 dielectric.

Dielectrics	Particle Size Distribution, µm			Surface Area, m^2/g	Powder Density, g/cm^3	RoHS Compliance
	D_{90}	D_{50}	D_{10}			
VLF-101	0.85	0.47	0.30	6.46	5.73	Yes

To perform microstructural and electrical characterization of VLF-101, .0805-type MLCC chips with 22 active dielectric layers and three different active dielectric (AD) layer thicknesses were fabricated using a traditional tape-cast process of solvent-based slips formulated with PVB-type binder. The VLF-101 dielectric was cast into tapes with about 12 microns green thickness. One, two or four green ceramic tapes were stacked together per each dielectric layer. The 95%Ag/5%Pd-based internal electrode paste doped with a small amount of ceramic inhibitor was used to make internal electrodes in all MLCC chips. The MLCC's were then subjected to a 48 hour binder burnout cycle (T_{max} = 400°C) and sintered at both 960°C/5hours and 975°C/5hours. A 10°C/min heating rate in air and open zirconia setters were employed to sinter the MLCC chips. Sintered chips were terminated using a platable Ag paste, followed by nickel-tin plating.

The sinterability and coefficient of thermal expansion of VLF-101 were measured by a differential high resolution dilatometer (model Dilatronic II, Port Washington, NY, USA) using a constant heating rate of 5°C/min to 1100°C in air. A scanning electron microscope (SEM, model ISI-100B, International Scientific Instruments, Pleasanton, CA,

USA) equipped with an energy dispersive spectroscope (EDS, model PGT XS169, Princeton Gamma-Tech, Princeton, NJ, USA) was used to analyze the overall microstructure of the sintered MLCC chips, their AD thickness, as well as to estimate the compatibility of high silver content internal electrodes with the VLF-101 dielectric. Temperature coefficient of capacitance (TCC) and dissipation factor (DF) with and without dc-bias were measured by a Multi-Frequency Precision LSR meter (model HP/Agilent-4284A, Santa Clara, CA, USA) at both 1kHz and 1MHz frequencies, with 1Vrms over the temperature range from -55°C to 350°C using two environmental chambers – one capable of operating from -55°C to 200°C and the other from 25°C to 400°C. A dc-bias of 300V was applied by a programmable DC power supply (model Sorensen DLM 300-2, Ametek, Inc, San Diego, CA, USA). The TCC/VC data was averaged based on groups of four identical MLCC chips. For the ultimate breakdown voltage (UBV) measurements, each MLCC chip was flashed at 50Vdc and the voltage was slowly increased until the sample failed. The current was limited to 50mA. Measurements were performed using a special high voltage power supply (model PS-1067, Sprague Specialties, Co, North Adams, MA, USA) capable of providing 3000Vdc. The average UDV was estimated based on groups of twelve identical chips. The dielectric breakdown strength (DBS) was estimated by dividing UDV by dielectric thickness. To compare reliability of MLCC chips with different AD thicknesses, highly accelerated life test (HALT) was performed at 180°C using a constant electric field strength, 13.5V/μm, for at least 100 hours. The HALT was performed using a commercially available HALT system (model 1025, Micro Instruments, Co, Canton, TX, USA). A total of 20 Ni-Sn plated MLCC chips per group were used in each HALT run. The leakage current of each capacitor was monitored during the test by measuring the voltage across 100kΩ resistors in series with the devices. A capacitor was considered failed when there was at least two orders of magnitude increase of voltage across the resistor. An additional LIFE test was performed on chips with around 20μm AD thickness at 125°C/300V test conditions for at least 2000 hours.

Results and Discussion

In general, any air-fired dielectric materials are characterized by a group of properties, the most important being dielectric sinterability and compatibility with Ag/Pd-based electrode systems, temperature coefficient of capacitance and dissipation factor with and without applied dc-bias, dielectric breakdown strength, insulation resistance, and life time, or dielectric reliability. In this study, we measured these properties on MLCC chips with different AD thicknesses to comprehensively evaluate the newly developed VLF-101 dielectric. In addition, some of the key properties were measured at temperatures up to 350°C, in the effort to estimate high temperature dielectric performance.

Dielectric Sinterability and Ceramic Microstructure

Sinterability of VLF-101 COG dielectric (in a pressed pellet form) is presented in Figure 1 as a temperature dependence of linear shrinkage and linear shrinkage rate during sintering with a constant heating rate of 5°C/min to 1100°C in air. According to the analysis, the dielectric actively sintered in a temperature range from 775°C to 1025°C. It is important to note here that the densification rate remained more or less constant, around 0.13%/min, within a wide temperature range from 825°C to 975°C. This result was confirmed by sintering several VLF-101 pellets with slightly different green densities and by the comparison of densification kinetics of different dielectric compositions [6]. We believe that the phenomenon of sintering with constant densification rate, exhibited by VLF-101 dielectric, is attributed to its chemical composition and not to the pellet preparation process. The constant densification rate during sintering is generally considered as a positive factor. First of all, it may affect an open porosity network microstructure, which, in turn, controls grain growth [7]. During the final stage of sintering (around 90% theoretical density), the open porosity network loses stability, forming closed spherical or ellipsoidal pores, which are located in triple junctions. Splitting and localization of spherical pores are accompanied by extended grain growth. Sintering with a constant densification rate (irrespectively of how it was achieved, either by the control of heating rates, or by the control of diffusion rates via material chemistry), may keep pore channels open up to higher densities (92-96%), resulting in more uniform microstructure [8, 9]. In addition, in multilayer

structures, constant densification rate of the ceramic may reduce mechanical stresses, which generally form between dielectric and electrode layers, due to differences in their densification rates. [10].

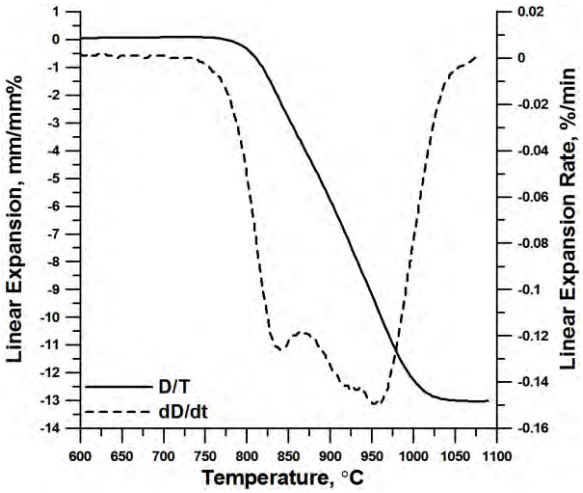


Figure 1. Temperature dependence of linear expansion and linear expansion rate of VLF-101 dielectric during sintering with constant linear heating rate in air.

Figure 2 shows a set of SEM microphotographs of a cross-sectional view of VLF-101 MLCC chips with different AD thickness, sintered at 960°C/5h. All three groups of chips, made with different thickness of dielectric layers, revealed dense and uniform ceramic microstructure with average grain size around 0.6-0.8 microns and estimated density of ceramic exceeding 98%. The estimated average grain size is in good agreement with the initial particle size distribution of the dielectric powder (Table 1), suggesting that the grain growth was very limited (less than 50%). Based on this information, it is reasonable to speculate that this dielectric may be potentially used in MLCC chips with dielectric layer thicknesses as low as 2-3 microns and still assure several dielectric grains across an active dielectric layer to ensure reliability [11]. EDS elemental analysis did not reveal any diffusion of Ag ions into the dielectric, or the formation of secondary phases at interfaces between dielectric and electrode layers, confirming that VLF-101 is compatible with high silver content internal electrodes.

Basic Dielectric Properties

Table 2 summarizes sintering conditions, fired density, active dielectric layer thicknesses and basic dielectric properties of all three groups of MLCC chips measured at room temperature. Figure 3 shows the effect of AD thickness and dc-bias on TCC behavior in the temperature range from -55°C to 125°C. VLF-101 dielectric exhibited very stable TCC behavior, well within COG specification irrespective of AD thickness, MLCC capacitance and applied dc-bias. The EIA specification for Class-I COG-type dielectrics is: $\Delta C/C$ must be within ±30ppm/°C between -55°C and +125°C, DF < 0.1%. Contrary to Class-II-type dielectrics based on ferroelectric compounds where the reduction of AD thickness generally leads to a clockwise rotation of TCC curve and considerable increase of dielectric constant, VLF-101 exhibited a very minor (a few ppm/°C) counter-clockwise rotation accompanied with a negligible reduction of dielectric constant. This phenomenon may be related to residual stresses, formed during cooling stages of sintering, due to differences in the coefficient of thermal expansion (CTE) of adjacent layers. The measured CTE of VLF-101 and 95%Ag/5%Pd-based electrodes in the temperature range of 200°C to 600°C was determined to be about 9.08μm/m*K and 16.74μm/m*K, respectively. Higher CTE of electrodes leads to the formation of significant compressive stress in dielectric layers. In addition, the residual compressive stress in MLCCs has a tendency to increase with decreasing of AD thickness. In Ni-$BaTiO_3$-based MLCCs with AD thickness around 1-2μm, the residual stress was estimated to be around 200-600MPa [12, 13]. In Class-I linear

dielectrics with ionic polarization, the compressive stress suppresses ion mobility, resulting in the reduction of dielectric constant and counter-clockwise TCC rotation [14]. In Class-II dielectrics based on ferroelectric materials with dipole polarization, however, this effect is hidden by a more prominent effect of increasing of dielectric polarization due to dipole growth with compressive stress [14].

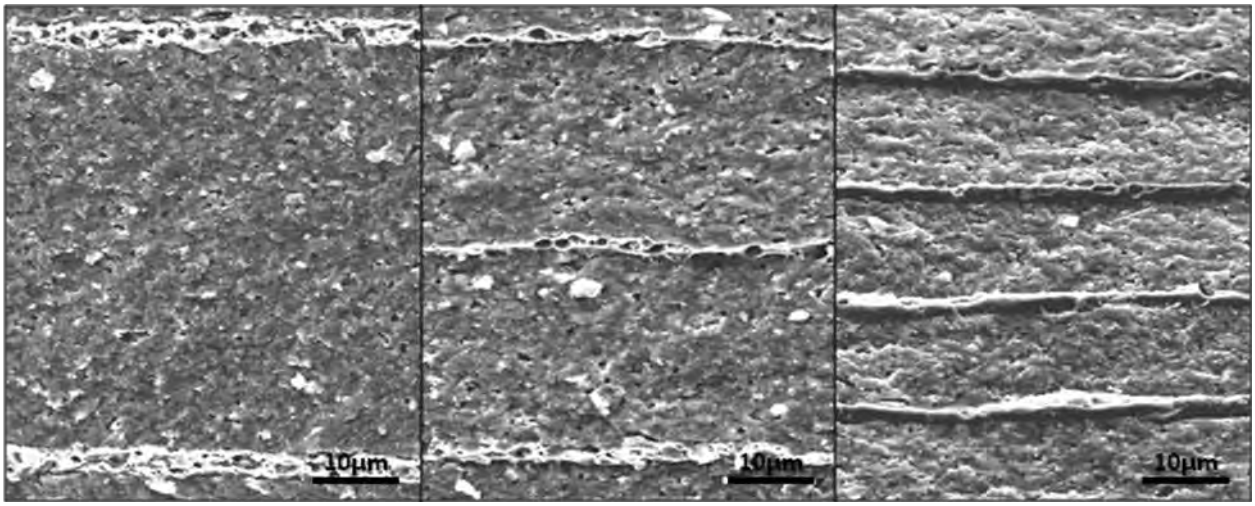
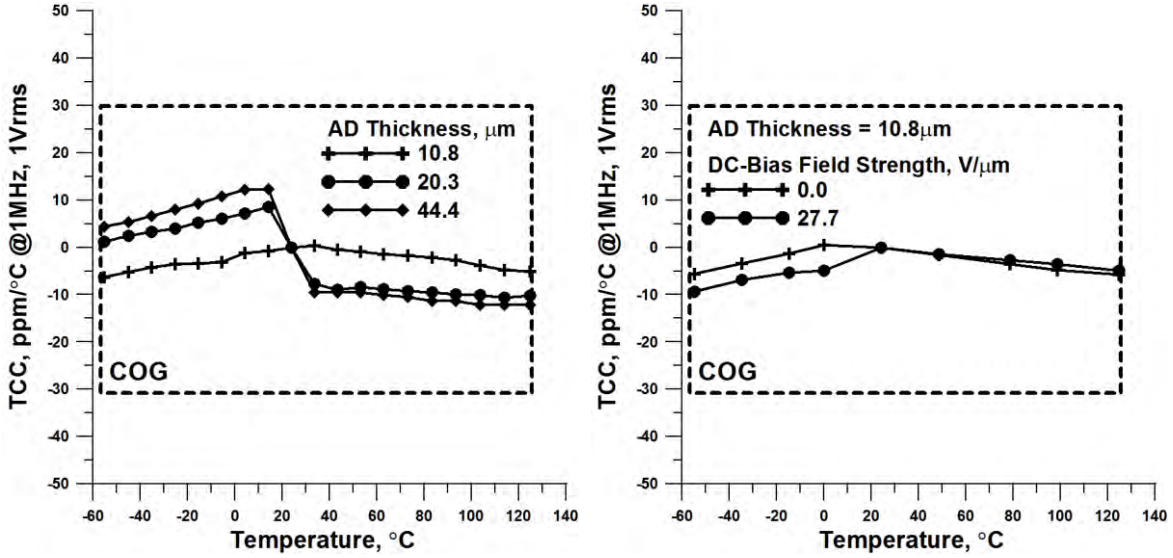


Figure 2. SEM microphotographs of VLF-101 MLCC chips sintered at 960°C/5h.

Table 2. Summary of basic dielectric properties of MLCC chips measured at room temperature.

Number of Stacked Ceramic Tapes per Dielectric Layer	Sintering Conditions	Fired Density, g/cm^3	Active Dielectric Layer Thickness, µm	Average Capacitance, pF @1MHz, 1Vrms	Average Dissipation Factor, % @1MHz, 1Vrms	Estimated Dielectric Constant	Average Dielectric Breakdown Strength, Vdc/µm
1	960°C/5h	5.66	10.8	1297.6	<0.01	99.4	138.8
	975°C/5h	5.74	10.6	1302.1	<0.01	99.6	118.5
2	960°C/5h	5.66	20.3	628.8	<0.01	99.9	92.5
	975°C/5h	5.74	20.1	632.4	<0.01	100.3	82.1
4	960°C/5h	5.67	44.4	285.4	<0.01	100.5	59.6
	975°C/5h	5.74	44.2	291.6	<0.01	100.7	53.2

The effect of AD thickness and sintering conditions on dielectric breakdown strength is shown in Figure 4. DBS of VLF-101 exhibited a significant increase from about 60Vdc/µm in MLCCs with 44.4µm AD up to almost 140Vdc/µm in MLCCs with 10.8µm AD thickness. This behavior is well known in the industry and is generally attributed to better heat dissipation and a lower amount of flaws in MLCCs with thinner dielectric layers [15-17]. It is also well known that DBS generally decreases with increasing soak temperature or time, mainly due to redistribution of sintering flux along grain boundaries and/or evaporation of some constituents from the composition [18]. In any case, VLF-101 revealed competitive DBS behavior compared to other dielectric materials [6, 15, 16, 19]. A very high stability of TCC curve vs. AD thickness and applied dc-bias accompanied with a high DBS makes the VLF-101 dielectric a good candidate for high voltage applications.



a b

Figure 3. Effects of (a) AD thickness and (b) dc-bias on TCC characteristics of VLF-101 MLCC chips, sintered at 960°C/5h.

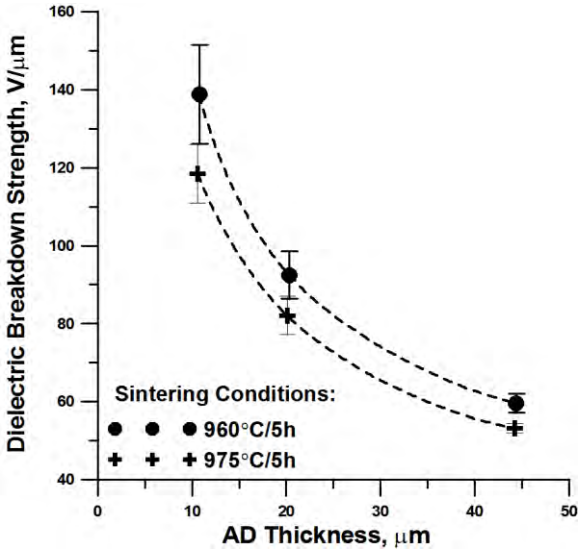


Figure 4. Effect of sintering conditions and AD thickness on dielectric breakdown strength of VLF-101 dielectric.

Dielectric Properties at High Temperatures

In order to evaluate high temperature properties of VLF-101, temperature coefficient of capacitance and dissipation factor with and without dc-bias were measured in the temperature range of room temperature up to 350°C, (Figure 5). Irrespectively of AD thicknesses and applied dc-bias, TCC behavior of VLF-101 remained well within COG limits of ±30ppm/°C, (Figures 5a and 5c). This behavior is in good agreement with high temperature properties of other high-K COG dielectrics, based on pseudo-tungsten bronze-type solid solutions [6]. It is interesting to note that low- and mid-K COG dielectrics, on the other hand, start to deviate from COG limits at lower temperatures [19].

The dielectric losses of VLF-101 remained below 0.1% up to approximately 230°C and did not exhibit any noticeable changes either due to variation of AD thickness or applied dc-bias (Figure 5c and 5d).

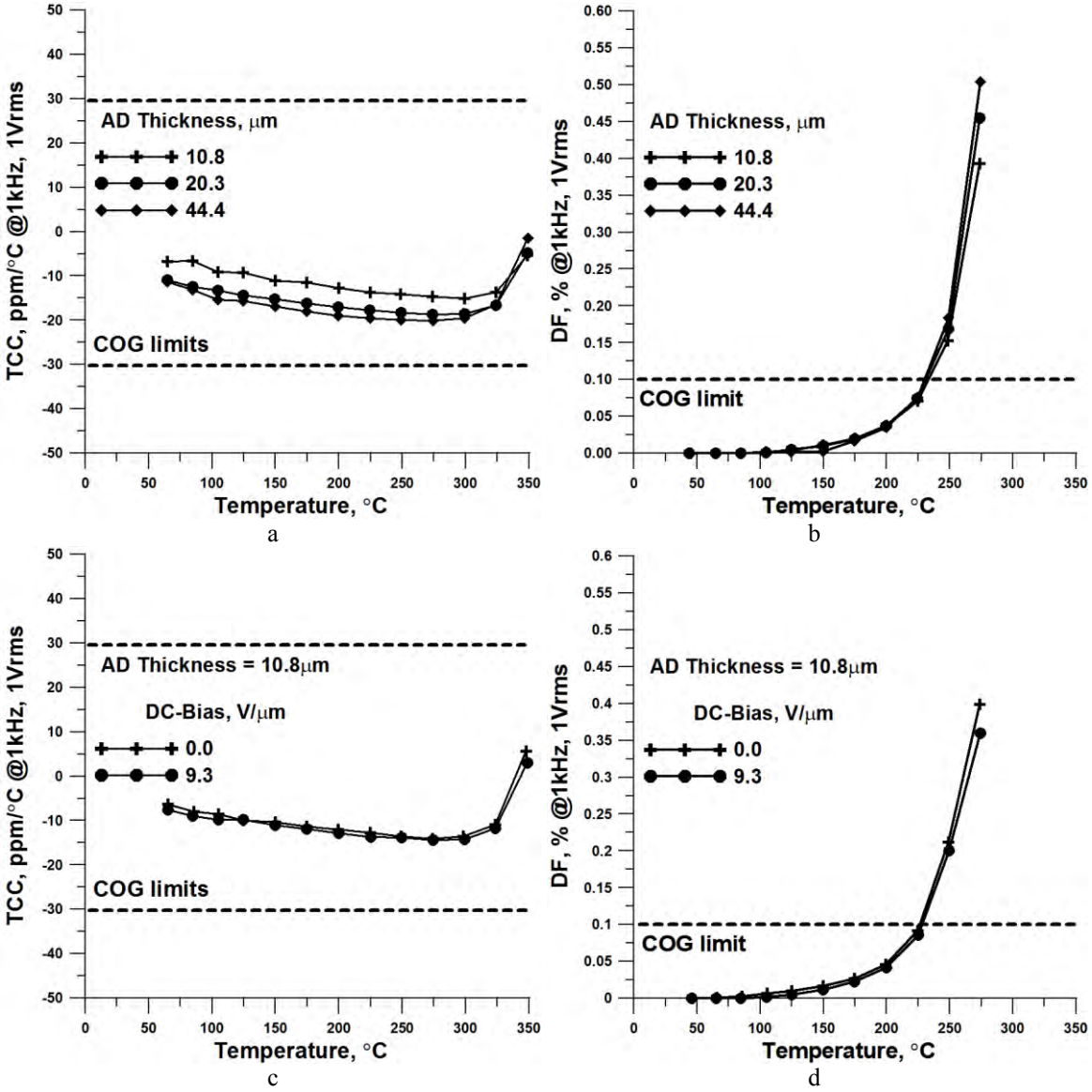


Figure 5. High temperature performance of TCC and DF of VLF-101 MLCC chips sintered at 960°C/5h vs. AD thickness and applied dc-bias.

Dielectric Reliability

Long term reliability of dielectric properties is a critical parameter of multilayer ceramic capacitors designed for the specialty capacitor market. To evaluate the reliability of VLF-101 dielectric, Ni-Sn plated MLCC chips with different AD thicknesses were subjected to highly accelerated life tests (HALT), performed at 180°C at a constant electric field strength of 13.5Vdc/μm, for at least 100 hours. As mentioned previously, 20 MLCC chips per group

were used for each run and a capacitor was considered failed when there was at least 2 orders of magnitude increase of voltage across the resistor. In addition, a group of MLCC chips with around 20µm AD thickness were subjected to a LIFE test at 125°C and 300Vdc for at least 2000 hours. Basic dielectric properties of the chips post LIFE test were compared with the properties of untested components. The results of HALT and LIFE tests are summarized in Tables 3 and 4.

Table 3. Reliability of VLF-101 chips sintered at 975°C/5h based on HALT and LIFE tests.

AD Thickness, µm	10.8	20.3	44.4
HALT test conditions	180°C/146Vdc/100h	180°C/274Vdc/100h	180°C/600Vdc/150h
IR after 2 hours, Ω	$1.9*10^{10}$	$5.6*10^{10}$	$1.1*10^{11}$
IR after 100 hours, Ω	$1.7*10^{10}$	$4.9*10^{10}$	$9.0*10^{10}$
Number of failures	0F/20	0F/20	0F/20
LIFE test conditions	N/A	125°C/300Vdc/2000h	N/A
IR after 2 hours, Ω	N/A	$> 3*10^{11}$	N/A
IR after 2000 hours, Ω	N/A	$> 3*10^{11}$	N/A
Number of failures	N/A	0F/20	N/A

Table 4. Comparison of basic dielectric properties of VLF-101 MLCC chips with 20.3µm AD thickness before and after 2000h of LIFE testing.

	Before LIFE test	After 2000h of LIFE test
Average Capacitance, pF @1MHz, 1Vrms	628.8	628.8
Average DF, % @1MHz, 1Vrms	<0.01	<0.01
TCC at -55°C/+125°C @1MHz, 1Vrms	N1/N10	N3/N10
Average DBS, Vdc/µm	92.5	100.9

Based on the results of both HALT and LIFE tests, VLF-101 dielectric did not exhibit any failures or degradation of dielectric properties at the abovementioned test conditions; suggesting its high reliability. More tests are required to establish application limits of the new dielectric.

Summary

An environmentally friendly (RoHS compliant) very low fired COG dielectric, VLF-101, was developed by MRA Laboratories, Inc. VLF-101 offers high dielectric constant, around 100, has the capability to sinter at a wide temperature range of 950°C to 1000°C, and is compatible with 95%Ag/5%Pd electrode systems. Comprehensive evaluation of its basic dielectric properties, performed on MLCC chips with different AD thicknesses in broad temperature and electric field ranges, confirmed that this dielectric can be used for value-added and application specific specialty capacitor markets, where high reliability of dielectric properties is critical. VLF-101 is a user friendly COG dielectric, which offers a high dielectric constant necessary for capacitance range extension and considerable savings in terms of compatible internal electrode compositions. Moreover, this dielectric can be used for high temperature applications up to 200°C and beyond, depending on the flexibility of electrical circuit board designs.

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