Dielectric Properties of a Newly Developed Very Low Fired COG Dielectric for High Q and High Voltage Applications

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Abstract:
A very low fired (VLF) dielectric material has been developed for high Q, COG MLCC applications and it has also shown good dc and ac high voltage capabilities. The dielectric properties are: dielectric constant (K) = 23±1; Q·*f* at 10GHz = 24750 (ceramic only), TCC = ± 30 ppm/°C, I.R. at 25 and 125°C > 1012 ohms, dc breakdown field > 100V/microns, ac breakdown field around 50 Vrms/micron.

This environmentally friendly composition is based on a modified magnesium zinc titanate system. It is compatible with aqueous, as well as PVB and acrylic binder systems and 95Ag/5Pd inner electrode materials.

I. INTRODUCTION

Significant efforts have been devoted to the development and characterization of various types of ceramic dielectric materials for microwave applications. These materials are largely used for wave guides, band-pass filters and antenna duplexers for microwave telecommunications (1,2). Many of these dielectric systems have to be sintered at relatively high temperatures (>1200°C), and the electrode terminations are usually applied after sintering.

In the case of multilayer ceramic capacitors (MLCC's), the dielectric and the electrode system must be considered as a single device. Therefore, the issues relating to co-firing and to the effect of the electrode resistance on the overall Q and equivalent series resistance (ESR) of the chip capacitor will add another dimension to the complexity of the system. The market demand for these capacitors to operate in the GHz range of the frequency spectrum prompted further research and development for higher Q dielectrics that could be sintered at relatively low temperatures (<950°C). A high silver content electrode, i.e. 95Ag/5Pd can be utilized for this application.

In this paper we will present the dielectric properties of a newly developed ceramic material based on a modified magnesium zinc titanate. The electrical results of some MLCC chips made from this material with 95Ag/5Pd inner electrode will also be described.

II. EXPERIMENTAL RESULTS

Commercially available powder, MRA product VLF-220, was used for this evaluation (3). The powder properties were as follows: particle size distribution; D_{90} = 0.82, D_{50} = 0.57, D_{10} = 0.37 micron; surface area = 4.03 M^2/gm and powder density = 4.11g/cm^3. Typical electrical properties of this dielectric in a 0805 chip capacitor are described in

Table 1.

Table 1
Basic Dielectric Properties of 0805 MLC Chips
with 95 Ag/5 Pd Internal Electrode
10.5 Layers at about 20 microns

Fired Density (Ceramic K-Square), g/cm^3	4.15
Capacitance, pf	65
"K"	23
D.F. at 1mHz, %	0.01
TCC, ppm/°C	
-55 to 25	11
25 to 125	23
Dielectric Breakdown Field, V/μ	110
I.R. (at 300V, 125°C, 1 hour), ohms	>3 x 10^{12}
I.R. (at 300V, 125°C, 1000 hours), ohms	>3 x 10^{12}

A. High Q Characteristics

1. Ceramic Substrate

Ceramic substrates (3.8 x 3.8 x 0.1cm) were fabricated by using a wet process method and fired at about 960°C, 5 hour soak. The fired density was about 4.16 g/cm^3, (>97% of theoretical density), and average grain size was between 1 and 2 microns. The Q measurements were performed at Penn State University, Department of Dielectric Studies, using a split-cavity resonance technique at 10 GHz frequency. A similar size Al_2O_3 substrate was measured at the same time, as a standard reference. The dielectric constant (K), quality factor (Q), and $f \cdot Q$ of both samples are shown in Table 2.

Table 2
Q Measurements at 10 GHz using
Dielectometer Model RMD-C-08

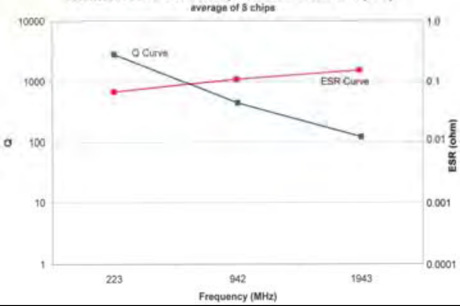
Sample	K	Q	f (GHz)	f·Q
Al_2O_3	9.04	1515	14.5	21968
VLF-220	21.05	2380	10.6	25228

Note: Measurements courtesy of Penn State University

2. Ceramic Chip Capacitor

A sample of 0603 chip capacitors with a series design (Figure 2d) was manufactured using the same wet deposition process and utilizing a 95Ag/5Pd inner electrode. These capacitors were sintered at 950°C, 5 hour soak. The electrical properties were: Capacitance at 1MHz, 3.8 PF, and D.F. <0.001%. The Q and ESR between 223 and 1900MHz were kindly measured by one of our MLCC customers, using a Boonton 34A Resonant Coaxiel Line System. The results are shown in Figure 1.

Figure 1
Q factor and ESR of 0603 MLC Chips 3.9PF, as a function of frequency
average of 5 chips

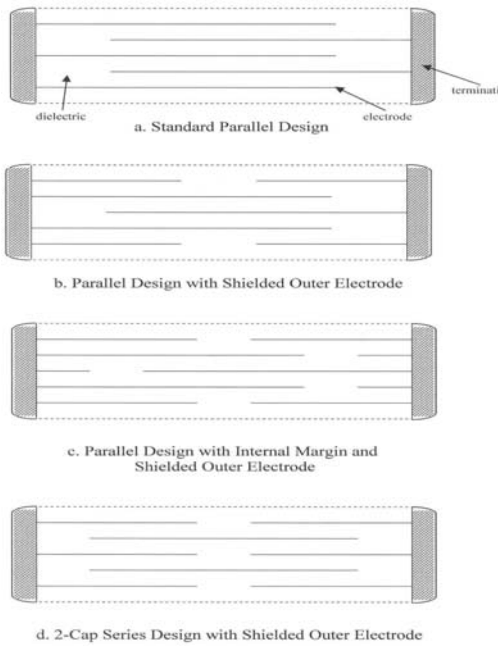


B. High Voltage Dielectric Breakdown Characteristics

Although this dielectric was mainly developed for high Q MLCC applications, it has also shown excellent dielectric breakdown voltage and thus could be used for low capacitance value high voltage MLCC applications.

For high voltage applications (>1000V), the chip design and electrode cofigurations become an important aspect for achieving the optimum performance of a given dielectric. Figure 2 shows some of the typical inner electrode designs that have been used for many years by the MLCC manufacturers.

Figure 2
Chip Design for High Voltage Applications

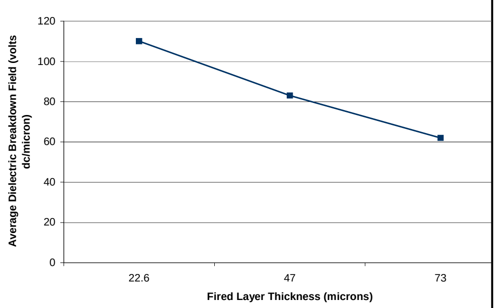


1. Effect of Dielectric Thickness on Dielectric Breakdown Field

To assess the voltage breakdown performance of this dielectric as a function of varying layer thickness, we manufactured and evaluated a series of 0805 chips with 10 active layers and layer thickness ranging between 21 and 73 microns, using a standard chip design configuration (Figure 2a).

These chips were made and fired at the same time. The inner electrode was the 95Ag/5Pd system. A sample of 20 chips from each of three different dielectric layer thicknesses were evaluated for ultimate dielectric breakdown. The chips were immersed in silicon oil during measurements. Figure 3 shows the average breakdown field in volts/microns and as a function of dielectric layer thickness. As can be seen from this curve, the breakdown field decreased by about 50% when the layer thickness increased by about three times. This phenomenum is very well known for most ceramic dielectrics and is believed to be attributable to the increase in the number of voids and/or defects per unit volume of the active layer.

Figure 3
Dielectric Breakdown Field as a Function of Active Layer Thickness



2. Series Capacitor Design

To take advantage of the higher breakdown field in thinner dielectric layer chips, a series capacitor design similar to that of Figure 2d is recommended. Although this design will significantly reduce the capacitance volumetric efficiency, the improvement in breakdown performance will be very beneficial, especially when other factors such as surface arcing become a major concern for lower breakdown voltage.

Other designs such as Figure 2c can also be utilized to ensure consistent margins (gaps between inner opposite polarities electrodes). Two groups of 1206 size chips with 6 active layers and about 32 microns fired layer thickness were made. Group A consisted of the standard parallel design (Figure 2a), while group B employed the series design (Figure 2d). These samples were manufactured and fired at the same time. A sample of 10 chips from each group was evaluated for ultimate dc and ac breakdown voltage in silicon oil. The results are summarized in Table 3.

Table 3
Dc and ac Dielectric Breakdown Voltage
MLC Sample – 1206, 6 layers at about 32 microns
Average of 10 Chips

	Standard Parallel Design (Figure 2a)		Series Design (Figure 2d)	
	dc*	ac**	dc*	ac**
Breakdown Voltage Across Chip	2843	1649	5944	3365
Average Breakdown Field, V/micron	89	51	92	53

* 500μA current limiting, ramp rate 1200V/sec.
** 5000μA current limiting, ramp rate 400Vrms/sec.
Note: Samples were submerged in Silicone Oil.

As can be seen from the data, the dc breakdown field for both designs was about the same, around 90V/micron, while the ac breakdown field was also the same at about 52 Vrms/micron. Clearly more work should be performed to compare the breakdown field of both designs with thinner active layers (i.e. 20 and 10 micron dielectric thicknesses).

III. DISCUSSION

High Q MLCC application

As we described in figure 1, the average Q of the MLC chip at 1.9GHz was significantly lower than that of the ceramic substrate, measured at the higher frequency of 10.6GHz. These results suggest that at higher frequencies, the contribution of the ESR of the electrodes is the predominant factor that is affecting the Q of the chip. Therefore, the selection of the metal, as well as the thickness and the geometry of the electrode, will require considerable attention in the design of the capacitor. Since most low temperature air fired dielectric systems utilize Ag/Pd alloys for the electrode, it would be constructive to examine the electrical resistivity curve of this binary system as a function of composition. Silver and Palladium metals form a complete solid solution. The curve of electrical resistivity as a function of composition in shown in Figure 4. Therefore, it is essential that the resistivity of the electrode be minimized, providing that the temperature of the solidus line of the Ag/Pd alloys is about 20 to 30°C higher than the sintering temperature of the MLCC.

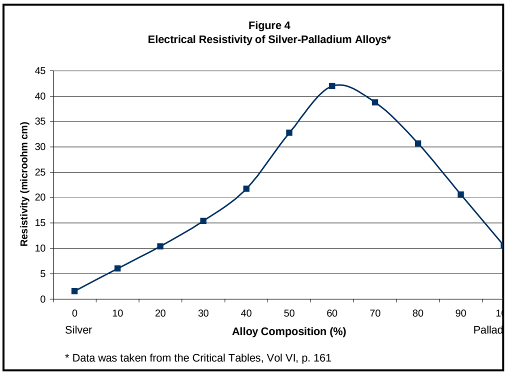
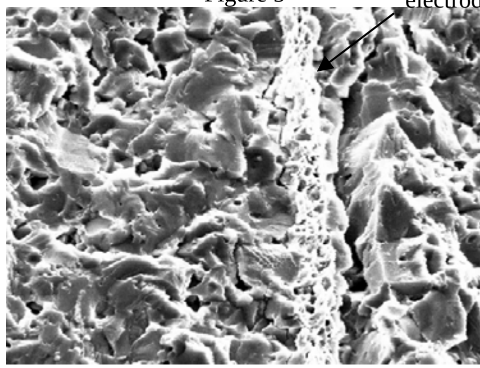


Figure 5



2500X Magnification

The electrode resistance is related to the resistivity of metal and geometry of the electrodes as follows:

$$R = \frac{\rho L}{A}$$

Where R = resistance of electrode (Ohms)
ρ = resistivity of the metal in micro ohm. cm.
L = length of electrode in cm.
A = cross section area of electrode (width x thickness) in cm^2.

From the above equation, it is apparent that reducing both ρ and L and increasing A will reduce R. Also, in the case of the MLCC, more layers in parallel will reduce R by a factor of 1/n, where n is the number of electrodes. Other considerations to minimize the ESR are: the contact of the electrode to the termination, as well as the termination, specifically those platable termination systems.
In the manufacturing of the MLC, it is very common to include a few percent of ceramic fine powder to the electrode to match the electrode shrinkage to that of the dielectric. The amount, type and particle size of the additives will increase the ESR. Figure 5 shows an SEM fracture cross section of the 0603 chips described previously.

In this case, a 4 w% of magnesium zinc titanate based powder relative to the electrode ink was incorporated in the electrode for shrinkage matching. As can be seen from figure 5, the electrode showed some voids where the ceramic powder has segregated during sintering and subsequently diffused into the dielectric. This type of electrode structure will also influence the ESR.

For the high voltage applications, many of the issues relating to electrode resistance, contact to the termination, and other factors will also influence dielectric breakdown. In particular, the charge and discharge currents for dc and ac applications should be limited to minimize the I^2R heating of the chips. We have examined many breakdown failures in various types of capacitors (COG and X7R) and observed localized electrode melting at the failure site. This effect was presumably caused by a localized instantaneous rise in the temperature at the failure site which has exceeded the melting temperature of the metal used in the electrode.

IV. SUMMARY

- An environmentally friendly very low fired dielectric ceramic powder with COG type TCC characteristics was developed for high Q and high voltage MLCC applications.
- The Q on a ceramic substrate at 10.6 GHz was about 2380 yielding $f \cdot Q$ of about 25228.
- A 0603 chip capacitor with 95Ag/5Pd with a capacitance value of about 3.8PF showed a Q and ESR of 120 and 0.145 ohm respectively, when measured at 1.9 GHz.
- The dc dielectric breakdown field in an 0805 chip with 10.5 active layers of 20 micron fired thickness was about 110V/micron.
- The ac dielectric breakdown field was about 52 Vrms/micron.
- The insulation resistance at 25 and 125°C when measured at 300 volts was greater than 10^{12} ohms.

- For higher voltage applications greater than 1000 volts, it is recommended that a series type chip design with non-active outer electrodes be utilized.
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7. REFERENCES

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