Effect of Dielectric Thickness on the dc and ac Dielectric Breakdown Field for Low Fired COG and X7R Capacitors

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ABSTRACT: Multilayer Ceramic Capacitors (MLCC's) are widely used in switched mode power supplies and other demanding high voltage dc and ac applications. In general, the breakdown field in terms of (V/μ) tends to decrease with increasing layer thickness. To gain some insight into this phenomenon, three different types of low fired 0805 MLC chips with varying layer thicknesses were studied. The dielectric materials consisted of X7R – K3500, COG – K85, and COG – K22. For dc application, the breakdown field strength (E_{dc}) was the highest for K3500 and K85, around 150V/μ for 20 micron layers, decreasing to about 75V/μ for 60 micron layers. The K22 chips showed a lower E_{dc} ranging from 110V/μ to 60V/μ, for layer thicknesses of 22 to 74 microns, respectively. It was determined that surface arcing was responsible for dc breakdown on those samples, which exceeded 4000 volts applied voltage. For ac application, the K22 chips showed a breakdown field strength (E_{ac}) higher than those of the K85 and K3500, ranging from about 60 Vrms/μ to 40 Vrms/μ for the different thicknesses. The K85 chips ranged from about 44 to 28 Vrms/μ while the K3500 chips ranged from 38 to 18 Vrms/μ. In the case of dc breakdown, it is believed that grain size and the amount of closed porosity are major factors affecting dc field strength, while for ac application at 50Hz, the dielectric losses, combined with closed porosity, are believed to be major factors affecting field strength.

Key words: Dielectric breakdown strength, dc, ac, low fired, X7R, COG, $BaTiO_3$, Magnesium Titanate, Neodymium- Barium-Titanate

INTRODUCTION

Advances in material processing, dielectric compositions, and manufacturing technologies for MLCC's have made significant impact on the utilization of these devices for high dc and ac voltage applications. Switched mode power supplies, pulsed power devices and numerous other high voltage miniaturized circuit designs continue to require even higher energy density chip capacitors.

It has long been recognized by many researchers that the dielectric breakdown field not only depends on the particular chemistry, microstructure, chemical homogeneity of the dielectric and several other factors, but to a significant extent, also depends on the total active area and layer thickness of the capacitors.

Lundstrom, et al. [1] showed that the dielectric breakdown field of single layer and laminate type structure TiO_2 capacitors decreased significantly with an increase in active area. Huebner, et al. [2] also studied the effect of layer thickness of a glass-TiO_2 composite in MLCC structures on the breakdown strength. They reported that the breakdown field of such a system decreased from about 700 KV/cm for a 0.02 cm layer to about 300 KV/cm for 0.12 cm thickness.

In our research [3], we have recently reported on the effect of layer thickness on the breakdown field of high Q, low fired COG capacitors. We found that the dc breakdown

field decreased from about 100V/μ for 22μ layer thicknesses to 50V/μ for 73μ layer thicknesses.

To gain further insight into this phenomenon, we have studied this effect in other low fired systems, including X7R and a higher K COG dielectric. This paper will describe preliminary results for dc and ac breakdown field for similar designs of chip capacitors.

MLCC SAMPLES STUDIED

0805 size X7R and COG chips were manufactured by the wet deposition process using commercially available products produced by MRA Laboratories. The powder properties of each dielectric are shown in Table I.

Table I

Powder Properties

Dielectric System	X7R (High K)	COG (High K)	COG (Low K)
MRA Product	VLF-342	LF-075	VLF-220Aq3
Particle Size (micron)			
D_{90}	0.97	1.13	0.86
D_{50}	0.47	0.57	0.55
D_{10}	0.30	0.36	0.37
Surface Area $M^2/gm.$	2.54	3.12	3.93

In each case, three different layer thicknesses ranging from about 20μ to 70μ with 5 active layers were manufactured. The cover coats (top and bottom) were about 375μ. Each group of chips were fired at the appropriate sintering condition for the dielectric.

A summary of the general properties of the 20μ chips is shown in Table II.

EXPERIMENTAL PROCEDURE AND RESULTS

About 75 chips from each group were silver terminated, fired, and tested for general electrical properties. A random sample of 10 chips from each group were used for dielectric testing. The ramp rate was set at 100V/Sec. and current was limited to 1500 microamperes. The ac test was performed at 50 Hz at the same ramp rate and current limiting to that of the dc test. All of the breakdown tests were performed with the MLC chips immersed in oil. The measurements were kindly performed by one of our valued MLCC customers.

Table II
General Properties of 0805
MLC Chips with about 20 microns active layer thickness

Dielectric System	X7R (High K)	COG (High K)	COG (Low K)
Electrode System	90 Ag/10 Pd	70 Ag/30 Pd	95 Ag/5 Pd
Ceramic System	Modified Fine Grain $BaTiO_3$	Modified $BaO.Nd_2O_3.TiO_2$	Modified $Mg_{2/3}Zn_{1/3}TiO_3$
Sintering Conditions	990/5 Hr.	1110/3 Hrs.	965/5 hrs.
% Theoretical Density	97	98.6	97
Capacitance (PF)	5700	120	29
Calculated "K" at 1KHz, 1Vrms	3600	88	23
D.F. %	1.2	0.0	0.0
TCC -55 to 25°C 25 to 125°C	 -1.4% -6.8%	 +18 ppm/°C -19 ppm/°C	 +6 ppm/°C +25 ppm/°C
I.R. at 15V/μ, 128°C, 24 Hrs.	$>10^{12}$ ohms	$>10^{13}$ ohms	$>10^{13}$ ohms

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Dielectric Breakdown Strength

Figures 1 and 2 show the average dielectric breakdown field (dc and ac) of 10 chips as a function of fired layer thickness for each dielectric group.

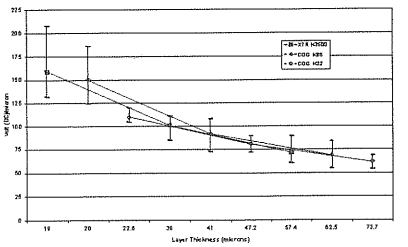

Figure 1: DC Dielectric Breakdown Field as a Function of Active Layer Thickness. 0805 – 5 Active Layers

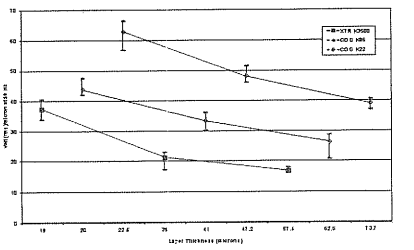

Figure 2: AC Dielectric Breakdown Field as a Function of Active Layer Thickness. 0805 – 5 Active Layers

Fired Microstructure

Figure 3 shows an SEM of the as fired surface microstructure of the X7R dielectric, while figures (4a, b, c) show a view of the fractured cross-section of the three different thicknesses. Similarly, figures 5 through 8 show the microstructure for the COG, high and low K, respectively.

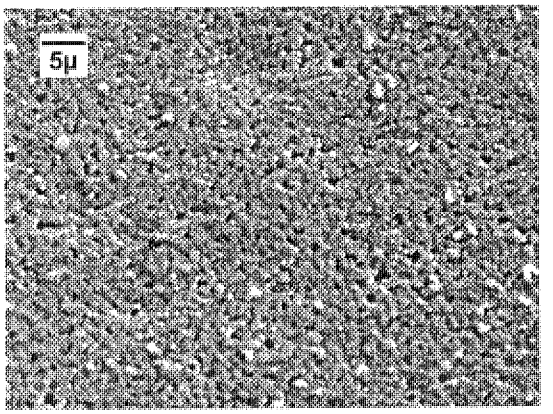

Figure 3: As fired surface of X7R MLC chip.

DISCUSSION

Although the same chip design was used for the three different dielectrics, the fired active area and layer thickness were slightly different due to the inherent difference in shrinkage of these materials. We have intentionally selected 0805 five layer chip designs to minimize the effect of the total active area and manufacturing defects on dielectric breakdown strength. However, this size MLCC started to arc across the surface when the dc voltage exceeded approximately 4000 volts.

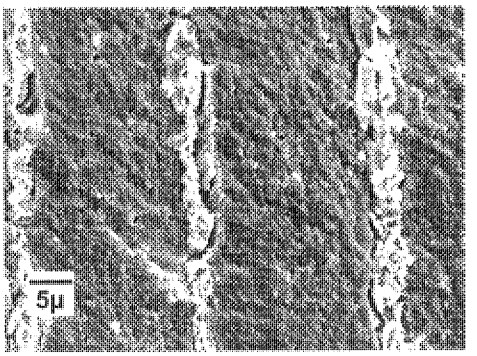

Figure 4a:Fractured cross-section of a 19μ section of a 39μ X7R MLC chip.

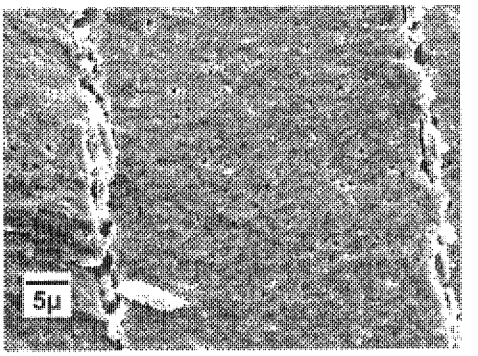

Figure 4b: Fractured cross-X7R MLC chip.

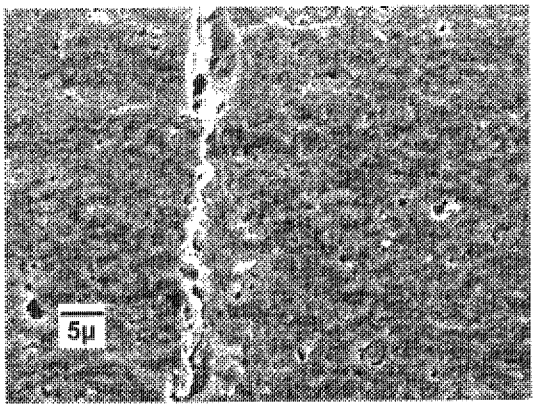

Figure 4c: Fractured cross-section of a 57μ X7R MLC chip.

dc Breakdown Field Strength (E_{dc})

In the case of the thinner layer design, the average breakdown for the X7R and K85 COG, were about 150V/μ, while that for K22 COG was about 110 V/μ. The lower value for K22 could be explained by the significantly larger grain size and large pores within grains and at triple points. However, as the layer thicknesses are increased to 40 and 60μ, the breakdown field decreased significantly to about 60V/μ. Although this phenomenon has been observed in the past, it was surprising to note that breakdown was nearly the same regardless of dielectric type, as layer thickness increased to over 40μ (see Fig. 1). Another set of samples from the 40μ and 60μ layer thicknesses of each of the dielectrics were coated with a protective layer of conformal coating material (manufactured by Electro Science Laboraties product code ESL-240-SB), cured to 150°C, and tested for dielectric breakdown. Similar results were observed to those described in figure 1. Evidence of arcing on the surface was observed in all of the groups. An additional group of samples of the same size without internal electrodes were produced. Again, arcing was also observed between 4400 and 5900 volts dc. In consideration of the results of each of these three experiments, it appears that the 0805 size chip should not be used in high dc voltage applications greater than about 3500 volts.

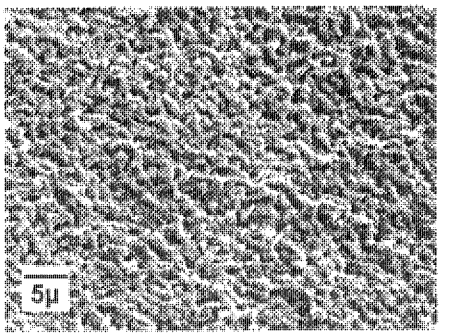

Figure 5: As fired surface of K85 COG MLC section of a 20μ chip.

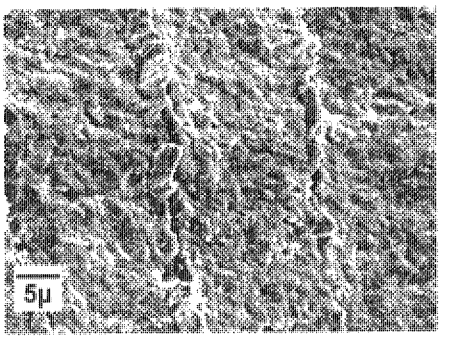

Figure 6a: Fractured cross- K85 COG MLC chip.

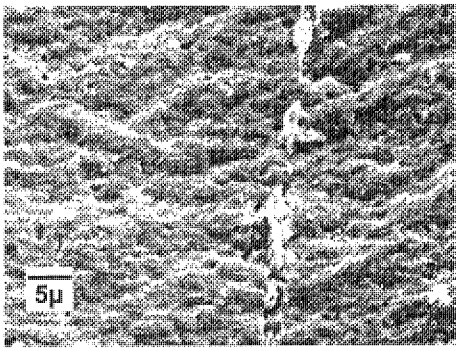

Figure 6b: Fractured cross-section of a 41μ K85section of a 63μ COG MLC chip.

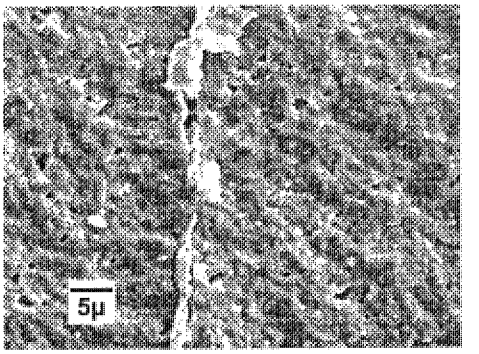

Figure 6c: Fractured cross-K85 COG MLC chip.

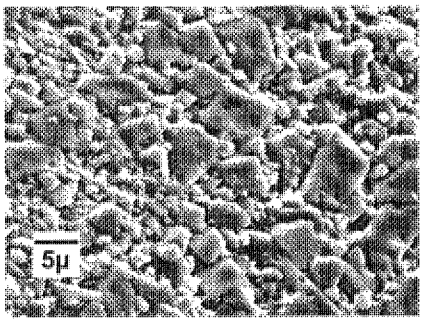

Figure 7: As fired Surface of K22 COG MLC section of a 23μ chip.

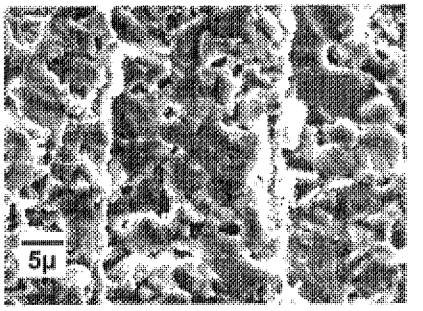

Figure 8a: Fractuerd cross-K22 COG MLC chip.

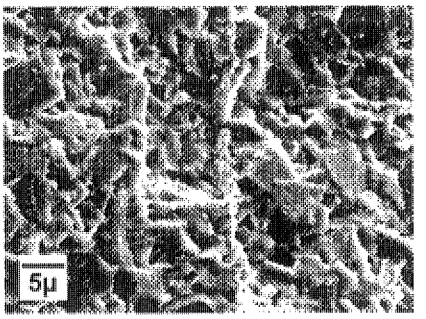

Figure 8b: Fractured cross-section of a 47μ section of a 74μ K22 COG MLC chip.

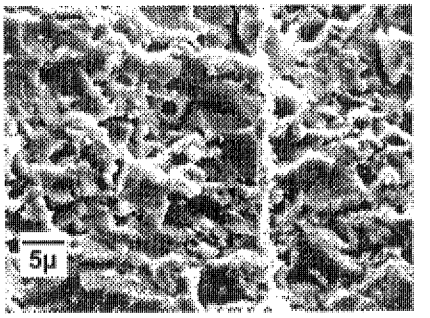

Figure 8c: Fractured cross-K22 COG MLC chip.

ac Breakdown Strength (E_{ac})

The comparative ac breakdown field strengths as a function of layer thickness for the three dielectrics are shown in Figure 2. Unlike the dc results, the COG K22 chips showed an E_{ac} of about 60 Vrms/μ for 22μ layers, decreasing to about 40 Vrms/μ for 73μ layers. The COG K85 chips showed an E_{ac} of about 43 Vrms/μ for 20μ, decreasing to about 27 Vrms/μ for 62μ layers. The X7R

K3500 chips showed an E_{ac} of about 37 Vrms/μ for 19μ layers, decreasing to about 17 Vrms/μ for 57μ layer thicknesses.

For a given thickness, the difference in the value of E_{ac} for the three types of materials can be related to the dielectric loss, where the quality factor Q of the X7R is significantly lower than those of the COG (i.e. Q K3500 < Q K85 < Q K22). Other contributing factors such as grain size and the number of closed pores will also influence the E_{ac} values.

Assuming that the major factor responsible for the initiation of ac dielectric breakdown is thermoionic in nature $(Irms)^2R$, then increasing the layer thickness will decrease the rate of heat dissipation. In turn, a thermal run-a-way environment is created in that specific spot of the layer which will ultimately cause the failure.

Since titanate based dielectrics are relatively poor thermal conductors, the most efficient path to conduct thermoionic heat generated in the chip to the outside are the internal electrodes. Therefore, an MLC design with multiple series capacitors at thinner layers may provide enhanced E_{ac} capabilities.

Effect of MLC Microstructure

As shown in figures 3 and 4, the grain size of the X7R K3500 chips was relatively small (< 1μ), with a transgranular fracture. The observed closed pores, generally classified as those greater than 1μ, are likely to be caused by manufacturing defects; while finer pores may be the result of insufficient sintering. Although we did not determine fired density of the MLC's with different layer thicknesses, examination of the thicker layers seems to indicate that closed porosity increased with increasing layer thickness. Perhaps at least in part, due to the fine grain microstructure, the high K X7R MLCC chips showed an extremely high E_{dc} (around 160V/μ).

To gain further insight into the possible mechanism responsible for the breakdown field of barium titanate based dielectrics, the current should also be monitored with increasing dc field, as suggested by Zhou, et. al. [4]. It is possible that at these high fields the initiation of breakdown can also be thermionic in nature.

In the case of the COG K85 chips, there was some grain growth with elongated grains with aspect ratios ranging from 3:1 to 4:1 (Fig. 5). The fractured microstructure is transgranular, with density estimated to be in excess of 98% theoretical (Fig. 6). As observed in the X7R chips, the frequency and size of the pores increased with increasing layer thickness. This dielectric has also displayed very high breakdown field, around 150V/μ for 20μ layer designs.

For COG K22 chips, there is significant grain growth during firing (Fig. 7). The breakdown field E_{dc} for 22μ layers was about 110V/μ. This is significantly lower than K3500 and K85 chips. It is believed that grain size may be the major cause for the lower breakdown field. The fractured microstructure is also transgranular (Fig. 8). Due to grain growth characteristics, the size of the pores (generally at triple points) tend to be larger than those of the other dielectrics. Some pores can also be seen trapped within individual grains.

SUMMARY

The dc and ac dielectric breakdown field strengths of three materials were studied in 0805 – 5 layer chip designs with various layer thicknesses. The dielectric materials consisted of low fired X7R K3500, COG K85 and COG K22.

The K3500 and K85 exhibited remarkably high dc breakdown fields of about 150V/μ for 20μ layers, decreasing to about 75V/μ for 60μ layers. The K22 showed a lower E_{dc}, about 110V/μ, decreasing to about 65 for nearly the same range of layer thicknesses.

Surface arcing on the 40 and 60μ layer thickness chips prevented the determination of the actual E_{dc} on these particular samples.

dc arcing was observed for 0805 chip capacitors, conformally coated capacitors, and those with no internal electrodes. In light of this, it would be advisable to limit the application of this size MLCC capacitor to about 3500 volts.

The K22 chips showed the highest ac breakdown field of about 63 to 39 Vrms/μ, followed by K85 of (43 to 28 Vrms/μ) and K3500 of (38 to 28 Vrms/μ) for layer thicknesses ranging from 20 to 70μ, respectively.

It is believed that the dielectric losses of these materials are the major factor for initiation of the ac breakdown field. The fired grain size, as well as the size and frequency of closed pores, are also believed to affect both dc and ac breakdown field strength.

ACKNOWLEDGEMENT

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