Electric Field Effects on the Insulation Resistance of Various Types of $BaTiO_3$ based X7R MLCC's at Elevated Temperatures

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Abstract:

Several types of $BaTiO_3$ based X7R multilayer ceramic capacitors, including Ni base metal electrode (BME), high fired 100% Pd precious metal electrode (PME), low fired with 70 Ag/30 Pd, and a new very low fired with 90 Ag/10 Pd were evaluated to determine the effect of varying dc electric field (E) on the insulation resistance (R) of these devices at elevated temperatures, (i.e. 130 to 160°C).

In each case, it has been found that the insulation resistance shows a straight line relationship when plotted as log R versus log E. This behavior suggests that the conduction mechanism is mostly space-charge-limited-current (SCLC).

The results of this study could be helpful for selecting the appropriate range of test voltages for various temperatures to better predict the life time and the reliability of the MLCC's as determined from the highly accelerated life test (HALT) conditions.

Key words: $BaTiO_3$, X7R, MLCC, BME, PME, HALT Reliability, high voltage, high temperature, space-charge-limited-current.

1. INTRODUCTION

During the past decade, significant advancements in materials and process technologies have made it possible to produce high volumetric efficiency X7R MLC capacitors. These devices are mostly of the BME type to minimize the cost of the chips in order to compete with and/or replace other types of capacitors (1). It is now a common production practice by some capacitor manufacturers to produce X7R MLC chips with hundreds' of layers as thin as 1.5 microns. While these high capacitance, small chip devices are targeted for commercial low voltage applications, <18 volts, we have also seen a strong drive in the opposite direction where similar types of dielectric materials are being used for high voltage, (>200 volts) and high temperature (> 125°C) MLCC applications.

As these materials and process technologies are being driven near their ultimate capabilities, the issue of the chip reliability and the demand for low reject rates in the PPM range has increasingly made many producers rely on HALT data to predict the useful life of the MLC for various applications. Furthermore, the HALT method has been very useful to compare the performance of chips made by different processes or utilizing different types of materials.

At MRA Laboratories, we have studied and reported the HALT performance of two types of low fired PME, X7R, MLC capacitors (2, 3). Other researchers have done similar studies on PME and BME type capacitors (4,5,6,and 7).

In these studies, the widely used and accepted empirical HALT equation was adapted (8).

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n \exp.\ \frac{E_a}{K} \cdot \left(\frac{1}{T_1} - \frac{1}{T_2}\right) \qquad (1)$$

Where:
t_1 = the mean time to failure at V_1 and T_1
t_2 = the mean time to failure at V_2 and T_2
V_1, V_2 = test voltages of the MLC, in Volts
T_1, T_2 = test temperatures of the MLC in °K
n = voltage stress exponent
E_a = activation energy (electron-volt)
K = Boltzman constant = 0.86×10^{-4} ev/°K

In our studies (2,3), we have found that the voltage stress exponent n varied between 5.4 and 7.1 depending on the test temperatures while the activation energy E_a increased from 1.1 to 1.35 v, with increasing voltage stress.

In the study reported by Randall, et al. (7) on very thin layer BME capacitors from various manufacturers, he also has shown a very wide range in the calculated values of n; 1.5 to 6.67 and E_a 1.34 to 1.50.

From equation (1), it is obvious that the predicted time to failure t_1 of a capacitor for a given test voltage and temperature will greatly depend on accurate and realistic values for both n and E_a.

It is against this background that the present study was undertaken to help to define the electric stress field regions at various temperatures for selecting accelerated test voltages in order to determine a conservative value for both n and E_a.

2. MLCC SAMPLES STUDIED

Six different types of $BaTiO_3$ based X7R chip capacitors were used in this investigation. They consisted of the following groups:

Group 1. 1206-69 nF high fired system with 100 Pd electrodes.

Group 2. 1206-71 nF low fired with 70 Ag/30 Pd electrodes.

Group 3. 1206-91 nF low fired with 70 Ag/30 Pd electrodes.

Group 4. 1206-98 nF very low fired with 90 Ag/10 Pd electrodes.

Group 5. 1206-103 nF BME with Ni electrodes.

Group 6. 0805-105 nF BME with Ni electrodes.

The BME chips of groups 5 and 6 were kindly provided to us by a leading MLC manufacturer. Other pertinent data for each group are summarized in table 1. The $BaTiO_3$ powders in groups 1 thru 4 were chemically prepared with controlled particle size and are employed in formulated compositions currently offered for commercial sale by MRA Laboratories. Groups 1, 2 and 4 use the same grade $BaTiO_3$ but employ different additives to accommodate the electrode system and sintering temperature. Groups 2 and 3 are nearly the same composition but with different grain size $BaTiO_3$. Table 2 shows the temperature coefficient of capacitance characteristics (TCC). All the groups appeared to show the core-shell type grain structure.

Table I
Summary of Basic Properties of Various X7R MLC Chips

Group	MLC Design	Capacitance Value at 1KHz, 1Vrms, 25°C (nF)	D.F. %	Fired Layer Thickness (microns)	Calculated °K	Grain Size of as Fired Surface (u)	Electrode System
1	1206	69	1.2	18.2	3300	0.4 – 0.5	100 Pd
2	1206	71	1.1	18.2	3650	0.6	70 Ag/30 Pd
3	1206	91	1.47	18.7	4600	0.9	70 Ag/30 Pd
4	1206	98	1.7	21.5	5400	0.5	90 Ag/10 Pd
5	1206	103	1.9	24	2200	0.2 – 0.3	100 Ni
6	0505	105	1.3	12.6	2300	0.2 – 0.3	100 Ni

Table II
TCC Characteristics
Average of three samples from each group were tested at 1 KHz, 1Vrms after 24 hrs. of aging.

Group	Temperature °C							
	-55	-15	25	45	65	85	105	125
1	7.5	1.2	0.0	-0.1	-4.0	-7.2	-6.8	2.0
2	+4.8	1.1	0.0	-0.3	-3.5	-6.5	-7.0	-1.3
3	7.5	1.6	0.0	-0.6	-5.5	-9.7	-11.4	-6.0
4	-9.1	-7.5	0.0	1.0	-4.0	-9.2	-12.9	-11.6
5	-9.0	-4.0	0.0	1.6	0.8	0.2	1.7	6.5
6	-7.3	-2.4	0.0	0.6	-0.6	-1.9	-1.6	0.3

3. EXPERIMENTAL PROCEDURE

10 to 12 chips from each group were tested at 130, 145 and 160°C. The oven temperature was kept to within ± 0.5°C from the set point. A 100K Ω resistor in series with each capacitor was used to monitor the leakage current during the test period. The test voltage was varied from 50 to 850V in 25 or 50 volt increments and was maintained to within ± 0.5 volts from the set point.

The leakage current was recorded after 5 to 7 minutes of electrification time. The steady state leakage current was achieved under one minute at test voltages greater than 150V.

The values of the leakage current at each test condition were within ± 5% for each test sample.

4. RESULTS AND DISCUSSIONS

Figures 1 thru 6 show the average insulation resistance (I.R.) expressed in ohm-Farad as a function of applied electric field (volts/micron). The active dielectric layer thicknesses of each group were measured as shown in table 1. This data represents an average of 4 to 6 chips. The measurements are believed to be accurate to ± 0.5 microns. The 25°C average capacitance values at 1KHz and 1Vrms were used to normalize the (I.R.) product in ohm-Farad. A more accurate representation of this product would be to use the capacitance value at the test voltage and temperature.

However, for this study, we have elected to follow the industry guideline.

Figure 1 shows the log of I.R. of group 1 as a function of the log of electric field (E) in volts/micron at the three temperatures. At 130°C the I.R. versus E displayed a straight line from about 30 to 56 V/micron. Below 25 V/micron the I.R. was relatively high, > 2 x 10^{10} ohms and it was difficult to achieve a steady state leakage current value.

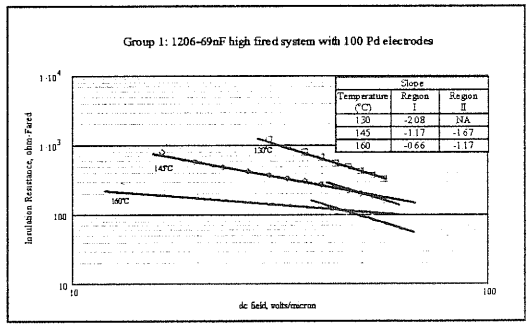

Figure 1

Straight line relationships were also observed at 145 and 160°C. However, the slope of the line (m) decreased with higher temperature and high field. A second anamoly in the conductivity appears to have occurred.

Figure 2 shows the log I.R. versus log E characteristics of group 2. In this case, the graphs showed nearly similar slope with no distinct change in slope at higher field.

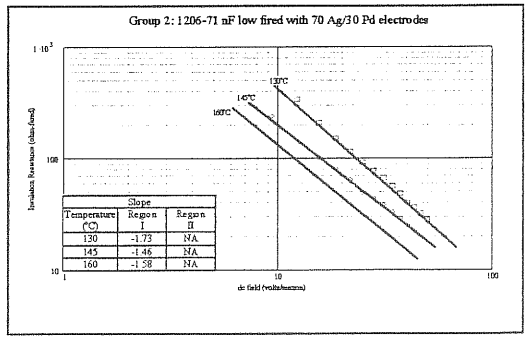

Figure 2

Figure 3 shows the log I.R. versus log E of group 3. Here again, straight line graphs were observed but with some change in the slope (m). The field where the slope of the conductivity has changed also decreased with increasing temperature.

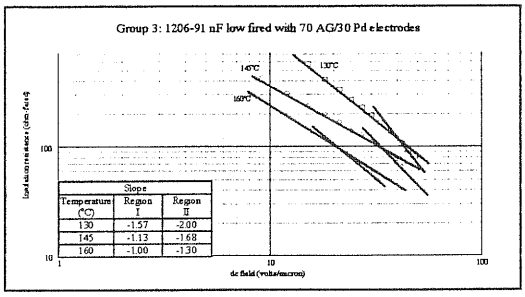

Figure 3

Figure 4 shows the log I.R. versus log E of group 4. The slope of the conductivity curve in region I decreased from about 2 at 130°C to 1.5 at 160°C. Since this group has a higher layer thickness, the voltage was not high enough to show the change in the conductivity at the lower temperatures (130 and 145°C).

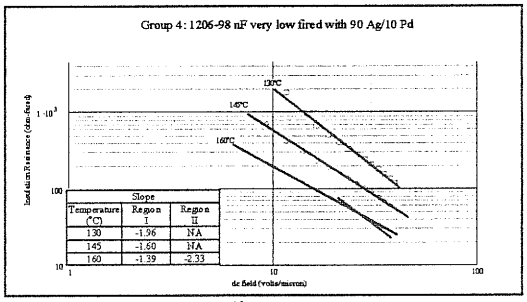

Figure 4

Figures 5 and 6 show the results of the BME chips of groups 5 and 6, respectively. Here again, the same anomaly in the conductivity characteristics was observed, but at lower electric field. In the case of group 5, the slope decreased from about 1.5 at 130°C to about 0.85 at 160°C. Where as in group 6, the slopes were a little greater, 2.1 at 130C, decreasing to 1.1 at 160°C.

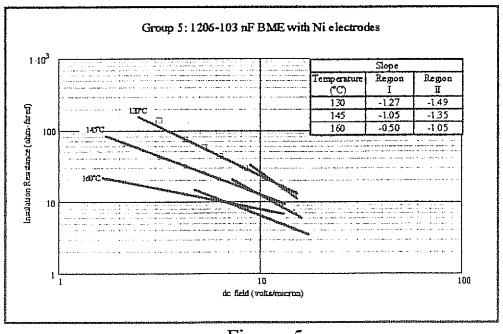

Figure 5

Figure 7 compares the curves of all the six groups at 130°C. Similar comparisons can be made for 145 and 160°C, but they are not shown here due to space limitations.

Figure 8 shows the I.R. as a function of 1/T for all the groups. The values of electric field (V/micron) were

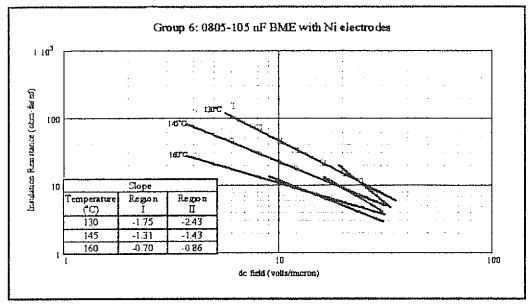

Figure 6

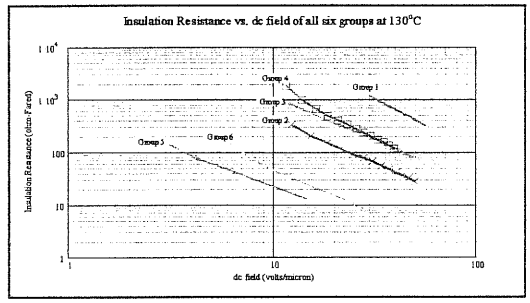

Figure 7

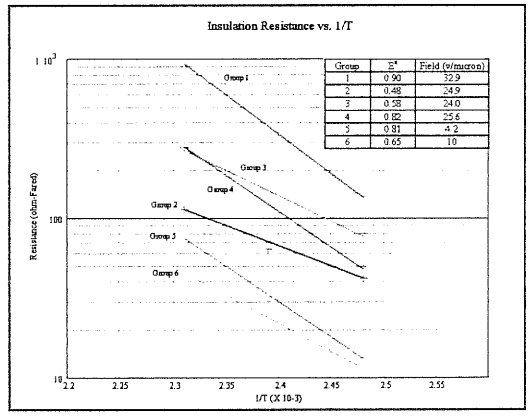

Figure 8

chosen to represent the results which are nearly in the middle of region I in the conductivity curves of figures 1 thru 6.

The decrease in I.R. with increase in temperature follows the Arrehenius relationship;

$$R = R_o \, EPX. (E/KT) \qquad (2)$$

where E is the activation energy of conduction. This should not be confused with the activation energy of failure shown in equation (1).

As can be seen from the above results, all the groups tested exhibited a straight line relationship between log R versus log E up to 160°C and maximum electric field. However, some change was observed in the slope at higher temperatures and fields.

These observations are consistent with conduction mechanisms described by Burton and others (1, 9).

For space-charge-limited-current (SCLC).

$$J = \frac{9\epsilon}{8d} \mu E^2 \qquad (3)$$

Where J is the current density, ϵ is the permittivity, d is the thickness of the dielectric, and E the electric field. A plot of log J versus log E would give a straight line with a slope of 2.

In some of the groups tested at 130°C, the slopes of log R versus log E was near 2. However, all groups showed a decrease in the slope with increasing temperature and field. These observations suggest that other conduction mechanisms start to take effect.

Accordingly, the use of the HALT equation (1) over a wide range of temperatures and voltages may lead to exceedingly high n and E_a which will greatly influence the predicted useful lifetime of the capacitor. Perhaps the HALT equation can be used more conservatively if limited to a specific temperature. As an example, for X7R, i.e. 130°C, the electric field can be selected within region I of log R versus log E. A HALT test at 2 or 3 voltages should give a conservative value for n. For X8R, similar HALT can be performed at 155 to 160°C and n can be calculated for that type of application. Perhaps a HALT test at the onset of the stress field from region I to region II for the various temperatures may prove to be useful. We will attempt to perform such a test in the near future.

5. SUMMARY

Various types of X7R MLC capacitors, including base metal and precious metal electrodes, were investigated at high temperatures (130 to 160°C) with increasing electric field, up to 55 volts/micron.

5.1 In all groups, the leakage current, or conversely the insulation resistance, showed linear relationship when plotted as log IR versus log E.

5.2 Two regions of conductivities, especially at higher temperatures and fields, were observed in some of the groups.

5.3 At 130°C, the slope of the curve in region I was near 2. This suggests that the conductivity mechanism is predominantly space-charge-limited-current.

5.4 The decrease in the slope of the region I conductivity curves with increasing temperature suggests that other conduction mechanism(s) begin to take effect.

5.5 The HALT equation can lead to unreasonable prediction of the useful lifetime of the capacitor if used over a wide range of voltages and temperatures. In such a situation, the slopes of the conductivity curves at the desired temperatures should be nearly the same in order for the HALT equation to accurately predict the useful life of the MLCC.

6. ACKNOWLEDGEMENT

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7. REFERENCES

1. Y. Sakabe, "Multilayer Ceramic Capacitors", Current Opinion in Solid State. Material Science edited by A.K. Cheetham, H. Inokuchi and S.J.M. Thomas. Current Chemistry Ltd. 2. pp 585-587, 1997.
2. G.H. Maher, "Highly Accelerated Life Testing (HALT) of K-4500 Low Fired X7R Dielectric", Dielectric Materials and Devices, pp 443-456, 2002.
3. G. H. Maher, et al., "Physical and Electrical Properties of a low fired K-3800 X8R Dielectric", Proceeding of the Tenth US-Japan Seminar on Dielectric and Piezolelectric Ceramics", pp 27-30, 2001.
4. L.A. Mann, et al., "Reliability of Base Metal Electrode Multilayer Ceramic Capacitors", ibid, pp 39, 41, 2001.
5. L.A. Mann, "Advances on Low-Fire Dielectric Technology for the Manufacture of MLCC and Comparison with Base Metal Electrode Technology", proceeding of the 9th US-Japan Seminar on Dielectric and Piezoelectric Ceramics, pp 281-287, 1999.
6. D.N. Donahoe, et al., "Failures in Base Metal Electrode (BME) Capacitors", 23rd Capacitor on Resistor Technology Symposium, pp 129-133, 2003.
7. M.S. Randall, et al., "Life Time Modeling of Sub 2 Micron Dielectric Thickness BME MLCC", ibid, pp 134-140, 2003.
8. T.P. Prokopowicz, et al., "Research and Development Intrinsic Reliability Subminiature Ceramic Capacitors", Final Report ECOM-9075-F, NTIS A0-864068, 69.
9. L.C. Burton, "Intrinsic Mechanism of Multi-layer Ceramic Capacitor Failure", Annual Report ONR Contract No. N00014-83-K-0168, 1986.